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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,299	11/05/1999	JAMES A. JOHANSON	JOHANSON79-3	3784

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EXAMINER	
ANYA, CHARLES E	

ART UNIT	PAPER NUMBER
2126	19

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/434,299	Applicant(s) JOHANSON ET AL.	
	Examiner Charles E Anya	Art Unit 2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3/ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1 – 4 and 6 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. 3,924,245 to Eaton et al. in view of U.S. Pat. No. 5,608,873 to Feemster et al.**

3. As to claim 1, Eaton teaches a shared memory processor-to-processor mailbox between at least two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: a shared memory accessible by a first processor and a second processor (Microprogram Store 11 Col. 6 Ln. 43 – 54), said shared memory including a first mailbox portion to pass data from said first processor to said second processor, and a second mailbox portion to pass data from said second processor to said first processor, said first mailbox portion (Stack 26/Stack 25 Col. 4 Ln. 7 – 22) and said second mailbox portion both being defined at least in part over common memory addresses (Microgrogram Store 11 Col. 4 Ln. 7 – 22), said first mailbox portion starting at a low physical address end of said shared memory, and addressably filling upward through to a highest physical address of said common memory ("...extend upwards..."

Col. 4 Ln. 7 – 22), said second mailbox portion starting at said high physical address end of said shared memory, and addressably filling downward through to said lowest physical address of said common memory ("...extends downwards..." Col. 4 Ln. 7 – 22).

Eaton is silent with respect to the first processor having write access to the first mailbox portion and not to the second mailbox portion.

Feemster teaches the first processor having write access to the first mailbox portion and not to said second mailbox portion ("...not write..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

4. As to claim 2, Eaton is silent with respect to the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said second processor has write access to said second mailbox portion and not said first mailbox portion.

Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said second processor has write access to said second mailbox portion and not said first mailbox portion ("...write-access..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

5. As to claim 3, Eaton is silent with respect to the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access to said first mailbox portion and not to said second mailbox portion.

Feemster teaches to the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access to said first mailbox portion and not to said second mailbox portion ("...read-access..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

6. As to claim 4, Eaton is silent with the shared memory processor-to-processor mailbox between at least two processors according to claim 3, wherein said second processor has read access to said first mailbox portion to said second mailbox portion.

Feemster teaches with the shared memory processor-to-processor mailbox between at least two processors according to claim 3, wherein said second processor has read access to said first mailbox portion to said second mailbox portion ("...read-access..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

7. As to claim 6, Eaton is silent with respect to the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said first mailbox portion and not to said second mailbox portion.

Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said first mailbox portion and not to said second mailbox portion ("...read-access...write..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

8. As to claim 7, Eaton is silent with respect to the shared memory processor-to-processor mailbox between at least two processors according to claim 6, wherein said second processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said second mailbox portion and not to said first mailbox portion.

Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 6, wherein said second processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said second mailbox portion and not to said first mailbox portion ("...read-

access...write..." Col. 4 Ln. 4 – 16). It would have been obvious to apply the teaching of Feemster to the system of Eaton. One would have been motivated to make such a modification in order provide read-write access to a mailbox (Col. 4 Ln. 4 – 16).

9. As to claim 8, Eaton teaches a method of utilizing a shared memory as a mailbox between two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: providing a contiguous block of shared memory (Microprogram Store 11 Col. 6 Ln. 43 – 54), allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory, allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end (Stack 26/Stack 25 Col. 4 Ln. 7 – 22), allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to said second physical address end ("...extend upwards..." Col. 4 Ln. 7 – 22), and allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to said first physical address end ("...extends downwards..." Col. 4 Ln. 7 – 22). Also see the rejection of claim 1.

10. As to claim 9, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 8, further comprising: assigning a minimum length to said first physical address end (Stack 26 Col. 4 Ln. 7 – 23).

11. As to claim 10, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 9, further comprising: assigning a minimum length to said second physical address end (Stack 25 Col. 4 Ln. 7 – 23).

12. As to claim 11, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 8, further comprising: reallocating a portion of a minimum length of said first physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said first processor (see figure 2, Col. 4 Ln. 7 – 22).

13. As to claim 12, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 11, further comprising: reallocating a portion of a minimum length of said second physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said second processor (see figure 2, Col. 4 Ln. 7 – 22).

14. As to claim 13, Eaton teaches an apparatus for utilizing a shared memory as a mailbox between two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: shared memory means for providing a contiguous block of shared memory means for allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory means for

allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end (Microprogram Store 11 Col. 6 Ln. 43 – 54, Stack 26/Stack 25 Col. 4 Ln. 7 – 22), means for allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to said second physical address end ("...extend upwards..." Col. 4 Ln. 7 – 22), and means for allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to said first physical address end ("...extends downwards..." Col. 4 Ln. 7 – 22). Also see the rejection of claim 1.

15. As to claim 14, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 13, further comprising: means for assigning a minimum length to said first physical address end (Stack 26 Col. 4 Ln. 7 – 23).

16. As to claim 15, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 14, further comprising: means for assigning a minimum length to said second physical address end (Stack 25 Col. 4 Ln. 7 – 23).

17. As to claim 16, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 14, further comprising: reallocating a portion of a minimum length of said first physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said first processor (see figure 2, Col. 4 Ln. 7 – 22).

18. As to claim 17, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 16, further comprising: means for reallocating a portion of a minimum length of said second physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said second processor (see figure 2, Col. 4 Ln. 7 – 22).

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. 3,924,245 to Eaton et al. in view of U.S. Pat. No. 5,608,873 to Feemster et al. as applied to claim 1 above, and further in view of U.S. Pat. No. 5,802,351 to Frampton.

20. As to claim 5, Eaton is silent with respect the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said shared memory is a dual port random access memory.
Frampton teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said shared memory is a dual port random

access memory (Dual Port Random Access Memory Device 31 Col. 3 Ln. 18 – 26). It would have been obvious to apply the teaching of Frampton to the system of Eaton. One would have been motivated to make such a modification in order to buffer data transfer between a MCU and DSP (Col. 3 Ln. 20 – 26).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,566,321 to Pase et al.

U.S. Pat. No. 5,414,826 to Garcia.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles E Anya whose telephone number is (703) 305-3411. The examiner can normally be reached on M-F (8:30-6:00) First Friday off.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles E Anya
Examiner
Art Unit 2126

cea

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